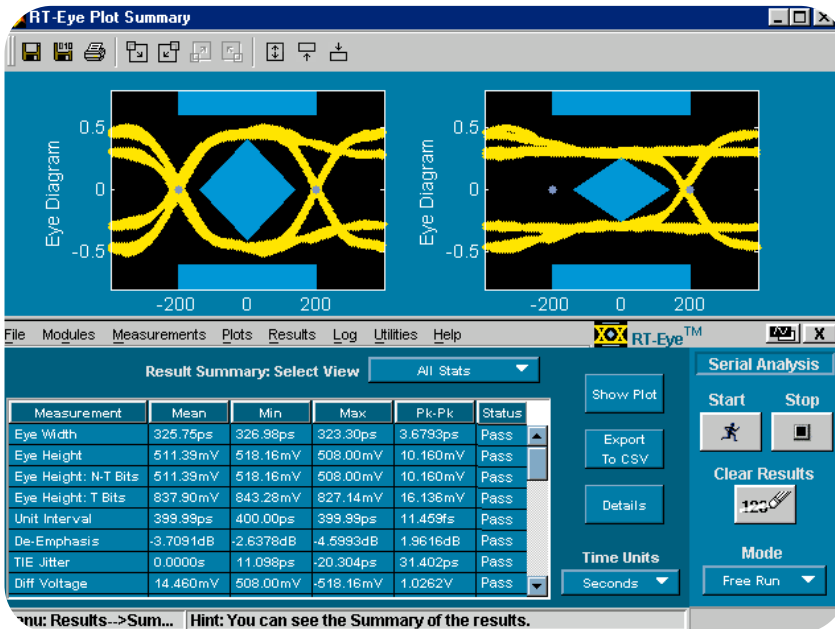# RT-Eye™ Serial Data Compliance and Analysis Software

▶ TDSRT-Eye

Accurate, Simple and Customizable Physical Layer Testing on Emerging Serial Data Standards Up to 3.2 Gb/s

When designing to industry standards, analog validation and compliance testing is critical to ensure device interoperability. RT-Eye Serial Data Compliance and Analysis software (Opt RTE) used with the TDS/CSA7000 and TDS6000 series of high-performance oscilloscopes, and proper probing solutions, provides the complete solution for analog validation and compliance testing of serial data buses.

▶ Applications

Analog Validation and Compliance Testing of Emerging Serial Data Standards Including:

PCI Express

InfiniBand

Serial ATA

Fibre Channel

10 GbE XAUI

10 GbFC XAUI

IEEE 1394b

RapidIO

▶ Features & Benefits

Real Time Acquisition and Analysis on Electrical Standards Up to 3.2 Gb/s

Real Time Eye (RT-Eye) Clock Recovery and Eye Rendering Provides:
– High Precision Eye Diagrams and Accurate Jitter Measurements*[1]
– Standard Specific Clock Recovery
– Pattern Length Verification for Jitter Measurement
– De-emphasis Measurements

Selectable Clock Recovery Algorithms That Model Receiver Device Behavior

SmartGating Feature for Flexible Clock Recovery and Measurement Windowing

Amplitude, Timing, and Jitter Measurements (including RJ, DJ, and Total Jitter @ 10^{-12} BER)

Automated Pass/Fail Waveform Mask and Measurement Limit Testing

Flexible Plotting and Export Tools for Further Serial Data Analysis

Multiple Graticule Plotting Windows for Simultaneous Eye Diagram, Trend, Histogram, Spectrum, and Bathtub Curve Analysis

Limits Module Feature for Customized Compliance Testing

Compliance Modules (Optional) Provide "plug-fest" Level Compliance Tests
– Available: PCI Express (Opt. PCE), InfiniBand (Opt. IBA)
– Other Standards: Under Development

Custom and Standard Specific Report Generation

Programming Interface for Test Automation via OpenChoice™ Software (GPIB and LAN)

*[1] Down to 700 fs RMS (TDS6000) and down to 1.5 ps RMS (TDS/CSA7000)

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RT-Eye™ Serial Data Compliance and Analysis Software

▶ TDSRT-Eye

Signal Integrity Starts at the Probe Tip

There are four fundamental probing approaches for high-speed signaling in differential serial buses. Active probing is required for probing live links on a circuit board. The use of two P7260 active probes provides a 6 GHz pseudo-differential solution that allows for the measurement of AC and DC common mode waveforms. The P7350 5 GHz active probe provides true differential measurement at the probe tip. For component and system compliance tests that require the serial link to be broken and terminated into 100 Ω differential, TCA-SMA connectors (provided standard on TDS6000 and TDS/CSA7000 series) provide a pseudo-differential solution. In order to take full advantage of the channel count and performance of your oscilloscope, the P7350SMA differential active probe is recommended. The P7350SMA probe provides single channel measurement for differential SMA connected test fixtures and devices, freeing up the other channels of the oscilloscope for additional testing. The P7350SMA also allows for simpler device test setup by allowing the use of a common mode termination voltage.

RT-Eye Clock Recovery and Eye Rendering

The first step in creating an eye diagram and performing accurate jitter measurements on data is recovering the clock from the serial bit stream. The RT-Eye eye rendering technique provides user selectable algorithms (PLL or Constant Clock) to recover the clock. This technique provides the following benefits:

High Precision Eye Diagrams – Since the waveform is captured from a single trigger event, and the clock is recovered through software, this method provides a much lower JNF than most Equivalent Time (ET) hardware-based clock recovery techniques.

Standard Specific Clock Recovery – PLL-based clock recovery is most common in many data communications standards. However, some standards such as PCI Express require supporting many receiver clock recovery topologies such as phase interpolation and oversampling. Software-based clock recovery allows you to select the clock recovery method that best suits your device. Further, use of the new SmartGating feature allows the user to define a "clock recovery window" within the acquisition as well as an additional "analysis window" that defines where in the recovery window the measurements will be made.

Pattern Length Verification –

To perform real-time jitter measurements such as Random Jitter (RJ), Deterministic Jitter (DJ), and Total Jitter (TJ) at 10^{-12} BER, a jitter test pattern length must be specified. The RT-Eye software lets you enter a pattern length or select from a number of popular jitter test patterns such as TS1, CJTPAT, CSPAT, CRPAT, etc. The software then verifies your device is transmitting a valid pattern length for the measurement.

De-emphasis Measurements – The real-time capture provides the ability to differentiate between transition bits and trailing bits for mask testing and measurements useful in systems employing De-emphasis (form of active equalization also known as Pre-emphasis or Equalization). Amplitude measurements can be made separately on the emphasized bits and the non-emphasized bits, allowing a De-emphasis measurement ratio to be displayed.

Waveform Eye Diagrams and Jitter Measurements are Inseparable

In the past, waveform mask testing and jitter measurements have been performed with at least two and sometimes three pieces of instrumentation. Waveform eye diagrams were viewed with sequential Equivalent Time (ET) sampling oscilloscopes or real-time oscilloscopes operating in a random ET mode.

Until the recent advent of real time jitter (RJ, DJ, and TJ @ BER) methodology in TDS oscilloscopes, BERT and/or Time Interval Analyzers were required to make Total Jitter measurements, using methods developed by data communications industry groups. More recently, some standards in the computer industry, such as PCI Express and Serial ATA, require that jitter measurements be performed on a specified number of consecutive (contiguous) bits, a requirement only satisfied by real-time oscilloscope technology. Whichever jitter measurement method is required, TDS RT-Eye software performs eye diagrams and various industry-specified jitter measurements from a single real-time waveform acquisition. Additional confidence can be gained by accumulating statistics over multiple acquisitions. This allows you to use a single high-performance real-time oscilloscope for design, debug, validation, and compliance of your serial data components.

Simple and Parametric Limits Modules

Mask testing and jitter measurements performed with TDS RT-Eye software can be turned into a custom compliance test by defining a Limits File and a User Mask File. A Limits File allows you to select which measurements you want to perform Pass/Fail compliance testing on. Test limits on masks and measurements can be edited and saved into User Mask and Limits Files.

Standard-specific Compliance Modules

TDS RT-Eye software can also be configured with optional Compliance Modules. Compliance Modules provide specific Pass/Fail waveform mask and measurement limit testing performed at industry-hosted "plug-fests." Compliance Modules currently available include:

InfiniBand Compliance Module – The InfiniBand Compliance Module (Opt. IBA), when ordered with TDS RT-Eye software, provides the complete solution for electrical compliance tests. Module includes physical layer measurements called out in Chapter 6 of version 1.1 of the InfiniBand architecture specification.

PCI Express Compliance Module – The PCI Express compliance module (Opt. PCE), when ordered with TDS RT-Eye software, provides the complete solutions for electrical compliance tests. Module includes physical layer measurements called out in Section 4.3 of version 1.0a of the PCI Express Base Specification.

Custom and Standard Specific Report Generation

Whether you're documenting results in the validation stage of your design or archiving compliance reports for future reference, the TDS RT-Eye software provides both standard compliance report templates and a Report Generator that allows you to customize your test reports.

▶ Characteristics

Bit Rates Supported – Up to [oscilloscope bandwidth (GHz)/1.5] Gb/s on 8B/10B encoded copper standards.

Measurements

Timing – Eye Width, Rise Time, Fall Time, Unit Interval, Bit Rate, Differential Skew.

Amplitude – Eye Height, Differential Voltage, High Amplitude, Low Amplitude, Common Mode DC Voltage, Common Mode AC Voltage, De-Emphasis.

Jitter – Jitter @ BER (RJ, DJ, TJ, and Jitter Eye Opening for a specified Bit Error Ratio), Jitter TIE (Data Time Interval Error).

Mask and Measurement Compliance Testing (Pass/Fail) – User definable mask geometries (User Mask) and measurement limit definition (Limits File). Masks and Limits hardcoded in Compliance Modules.

Clock Recovery – PLL (fc/1667 or custom), Mean, Median, Gated.

SmartGating – Provides up to two gated regions for clock recovery and measurement results. Gating Options – Cursors, Unit Intervals, Edges.

Population Control – Halts measurement accumulation on a specified Measurement Population or Number of Acquisitions.

Plots – Define up to four plots on multiple graticules. Plots can be viewed on instrument display or second monitor. Supported Plot Types: Unit Interval, Trend, Histogram, Spectrum, Bathtub Curve.

Worst Case Waveform Logging – Provides capture of worst case waveform for specified test condition.

Remote Control for Automation – The software can be controlled over GPIB or 100BaseT LAN connection. Windows and Unix remote operation is supported.

Online Help – Provides easy reference to standard test definitions.

Tektronix Oscilloscopes Supported

TDS6000 and TDS/CSA7000 series oscilloscopes (1.5 GHz models and above).

Recommended System Requirements

▶ Windows 2K OS (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. W2K).

▶ SDRAM (order upgrade 040-1682-00, 256MB DIMM module).

▶ 850MHz Processor (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. CPU).

▶ Version 2.4 Firmware (www.tek.com/site/sw/search/).

RT-Eye™ Serial Data Compliance and Analysis Software

▶ TDSRT-Eye

▶ Ordering Information

TDSRTE

RT-Eye™ Serial Data Compliance and Analysis Software Option.

Includes: Software on a compact disk, online documentation, and quick reference guide. Five-time free trial available to all supported instrument models.

When Ordering a New Oscilloscope:

Order from the options listed below.

When Upgrading an Existing Oscilloscope:

Order TDS6UP, TDS7UP, or CSA7UP with the options listed below.

Options

Opt. RTE – RT-Eye Serial Data Analysis software for TDS6000 and TDS/CSA7000 series oscilloscopes (1.5 GHz instrument models and above).

Opt. IBA – Requires Opt. RTE. Adds InfiniBand Compliance Software Module (4 GHz instrument models and above).

Opt. PCE – Requires Opt. RTE. Adds PCI Express Compliance Software Module (4 GHz instrument models and above).

Recommended Accessories

P7350 – 5 GHz differential probe.

P7350SMA – 5 GHz SMA input differential probe.

P7260 – 6 GHz single-ended probe.

P7240 – 4 GHz single-ended probe.

TCA-BNC – TekConnect®-to-BNC adapter.

AWG710 – Arbitrary waveform generator.

DTG5274 – Data timing generator.

Test Fixtures – Refer to www.tektronix.com/ serial_data for information on standard-specific test fixtures.

Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

CE   ISO 9001   GPIB

10/03   HB/SFI   55W-16615-3

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